REMARKS

Upon entry of the present amendment, claims 20, 21, 24, 28, and 33 will have been amended. In view of the herein contained amendments and remarks, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections and an indication to such effect in due course.

Applicants note with appreciation the Examiner's consideration and approval of the drawings filed September 13, 2000.

In the outstanding Official Action, the Examiner rejected claims 20-29, 33 and 34 under 35 U.S.C. § 102(b) as being anticipated by WADA (U.S. Patent No. 5,602,879). The Examiner further rejected claim 30 under 35 U.S.C. § 103(a) as being unpatentable over WADA in view of KANEMASA et al. (U.S. Patent No. 4,703,343) and further in view of ZHANG et al. (U.S. Patent No. 6,037,986). Finally, the Examiner rejected claims 31, 32 and 35 under 35 U.S.C. § 103(a) as being unpatentable over KANEMASA et al. in view of ZHANG et al.

Applicants respectfully traverse the above rejections and submit that they are inappropriate in view of the herein contained amendments and remarks.

One feature of the present invention, as generally recited in amended independent claims 20 and 33, is to estimate a first synchronization timing and a second synchronization timing of a received signal at sampling timings corresponding to multiple phases that vary

by 180°. From the first synchronization timing and the second synchronization timing, an estimated third synchronization timing is determined. In other words, a synchronization estimation of a received signal is utilized at two sampling timings corresponding to phases that vary from each other by 180°. Based on the results of these estimations, a definitive synchronization timing can be established.

In this regard, a sampling rate can be utilized in which eight samples, for example only, are taken per symbol, at a predetermined phase. After a certain number of symbols have been sampled, the phase of the sampling timings is shifted by 180° and samples are taken again at a rate of eight samples per symbol, for example only, at the shifted phase. The result is a synchronization timing estimation with a degree of time resolution equivalent to double the sampling rate.

This feature of the present invention has the advantage of enabling synchronization timing estimation with a higher degree of time resolution without substantially increasing the sampling rate of received signals. As a result, it is possible to reduce power consumption and cost.

In contrast to claims 20 and 33, WADA discloses a clock recovering circuit for digital modulation that detects a correlation between the levels of an output signal from a delay detection circuit at an adjacent pair of sampling points and setting one of the pair of the sampling points as a timing power. As shown in figure 11 of WADA, a phase shifter 96

shifts the phase in A/D converters 7 and 8 based on an output from the correlation judgment circuit 42. There is no disclosure in the WADA phase shifter 96 of synchronization timing estimation. Additionally, WADA does not disclose a third estimator that estimates a definitive synchronization timing estimation based on two synchronization timings such as recited in claims 20 and 33. Furthermore, WADA also fails to disclose or suggest shifting the phase of sampling timings 180°, as further recited in claims 20 and 33.

Accordingly, because WADA does not disclose, inter alia, a first estimator, a second estimator with a phase-shifted sampling, and a third estimator, the Examiner is respectfully requested to withdraw the rejection under 35 U.S.C. § 102.

WADA further fails to disclose or suggest inverting the polarity of a clock signal and thereby shifting the phase of sampling timings as recited by claim 21.

Thus, WADA fails to disclose or suggest the features of the present invention which include performing synchronization estimation of a received signal at sampling timings that correspond to synchronization timings as defined in the combination of claim 21.

Another feature of the present invention, as generally recited in independent claims 28 and 34, is the use of a table that stores operation value ratios in association with multiple short times. These operation value ratios are determined based on correlations between received signals and a known signal sequence. Using the table, the operation value ratio that is closest to the ratio of a correlation corresponding to a first synchronization timing of a low

accuracy is determined. A second synchronization timing of higher accuracy is set at a timing shifted from the first synchronization timing by the short time corresponding to the operation value ratio determined from the operation value table. In other words, the operation value ratio that is closest to a ratio of a correlation corresponding to a synchronization timing of low accuracy with reference to an operation value ratio table is selected. The operation value ratio and its respective short time sets a more accurate synchronization timing at a timing shifted from the less accurate synchronization timing by the short time corresponding to the operation value ratio.

Contrary to the recitations of claims 28 and 34, the WADA clock recovering circuit for digital modulation correlation refers to a correlation between the levels of an output signal from a delay detection circuit and is different from the correlation according to the present invention, which is measured between a received signal and a known signal sequence.

In particular, WADA samples a signal at a plurality of sampling points fixed in advance for each unit data cycle and detects correlations between each adjacent pair of the sampling points. In this regard, WADA does not disclose the operation ratio values of the present invention which are determined based on correlations. Thus, the correlation in the present disclosed invention is remote from the WADA correlation. Furthermore, estimating

synchronization timings of high accuracy with reference to an operation value ratio table is not taught by WADA.

WADA thus fails to disclose or suggest the above feature of the present invention which include setting a synchronization timing of high accuracy at a timing shifted from a synchronization timing of a less accurate synchronization by a short time corresponding to an operation value ratio, the short time being stored in a operation value ratio table as recited by claims 28 and 34.

In this regard, WADA does not disclose, inter alia, an operation value ratio table that stores operation value ratios in association with short times that in part determine a synchronized timing, and thus the Examiner is respectfully requested to withdraw the rejection under 35 U.S.C. § 102.

Another feature of the present invention, as generally recited in the combinations of independent claims 31 and 35, is to cancel inter symbol interference (ISI) using multiple tap coefficients prestored in association with short times. Furthermore, estimating a synchronization timing from the short time corresponding to the tap coefficient that maximizes the correlation operation result between a signal after interference cancellation and a known signal sequence. In other words, the above feature is to use multiple tap coefficients and cancel ISI from a received signal sampled at predetermined sampling timing, and set a synchronization timing at a timing shifted from the predetermined sampling timing

by the short time corresponding to the tap coefficient producing the maximum ISI cancellation result.

These features, inter alia, enable synchronization timing estimation with a high degree of time resolution that increases the order of the short times, without substantially increasing the sampling rate of received signals. As a result, it is possible to reduce power consumption and cost.

Contrary to claims 31 and 35, KANEMASA et al. discloses that the tap coefficients of an adaptive filter are sequentially corrected or updated by determining the correlation between the predicted residual ISI of a received signal. However, as the Examiner asserts in section 4 of the outstanding Official Action, the combination of WADA and KANEMASA et al. does not disclose using a look-up table to store possible tap coefficients. ZHANG et al. discloses storing possible tap coefficients in a look-up table.

However, the ZHANG et al. look-up table stores tap coefficients in association with motion detection metric, frame-wise motion activity measure, and edge detection metric (see column 12, lines 31-36). In this regard, the ZHANG et al. table does not have the features of the tap coefficient table recited in claims 31 and 35 of the present invention which stores tap coefficients in association with multiple short times. Moreover, the present invention is further distinguished from ZHANG et al. in that it cancels ISI using multiple tap coefficients stored in the tap coefficient table as further recited by claims 31 and 35. Moreover, the

present invention compares the ISI cancellation results corresponding to individual tap coefficients and acquires a synchronization timing.

Moreover, there is no suggestion or disclosure in WADA, KANEMASA et al. nor ZHANG et al separately or in any proper combination that render obvious the features of the present claimed invention including canceling ISI using multiple tap coefficients stored in a tap coefficient table and acquiring a synchronization timing using the tap coefficient that produces the maximum ISI cancellation result. Accordingly, the Examiner is respectfully requested to withdraw the rejection under 35 U.S.C. § 103.

Claim 21 has been amended into independent form and adds no prohibited new matter and is submitted to be allowable.

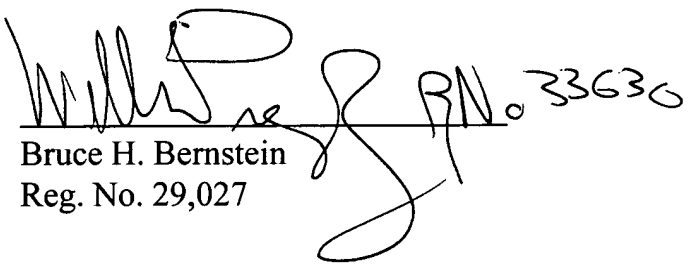
With regard to dependent claims 22-27, 29, 30, and 32, Applicants assert that they are allowable on their own merit and at least because they depend on one of independent claims 20, 21, 28, 31, 33, 34, and 35, which Applicants submit have been shown to be allowable.

Applicants have made a sincere effort to place the present application in condition for allowance and believe that they have now done so.

Any amendments to the claims which have been made in this amendment, and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

Should the Examiner have any questions or comments regarding this Response, or the present application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
Katsuaki ABE et al.



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